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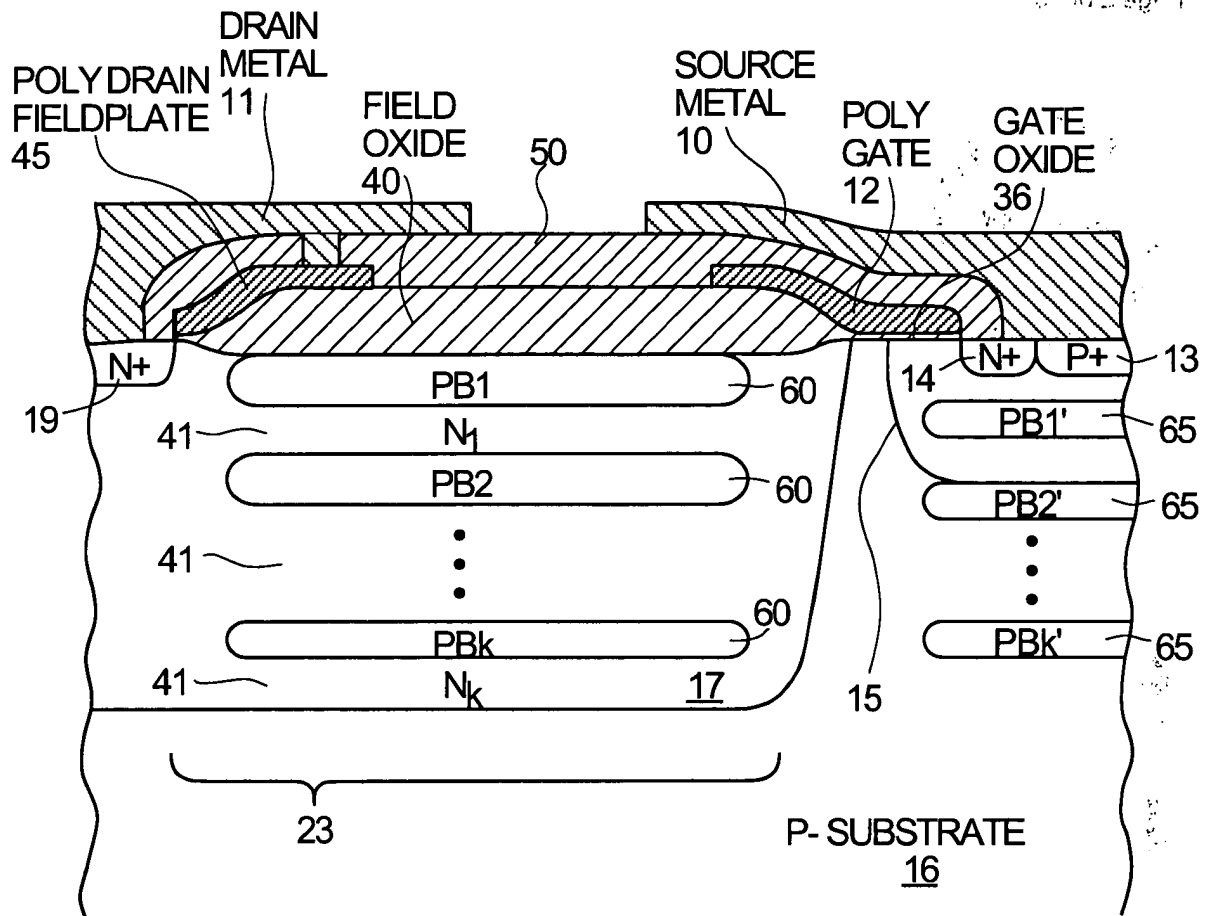
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FIG. 3



**FIG. 4**

FIG. 5 is a cross-sectional view of a transistor with a buried P-region. The transistor includes a substrate 16, a gate stack 12, a source region 10, and a drain region 11. The gate stack 12 is formed on the substrate 16 and includes a gate dielectric 12 and a gate electrode 26. The source region 10 is formed in the substrate 16 and includes a P+ region 13, an N+ region 14, and a P region 110. The drain region 11 is formed in the substrate 16 and includes an N+ region 19. A buried P region 18 is formed in the substrate 16 and is located beneath the gate stack 12. A P+ region 28 is formed in the substrate 16 and is located beneath the source region 10. A P region 35 is formed in the substrate 16 and is located beneath the P+ region 28. A P region 106 is formed in the substrate 16 and is located beneath the drain region 11. A P region 109 is formed in the substrate 16 and is located beneath the source region 10. A P region 23 is formed in the substrate 16 and is located beneath the gate stack 12.

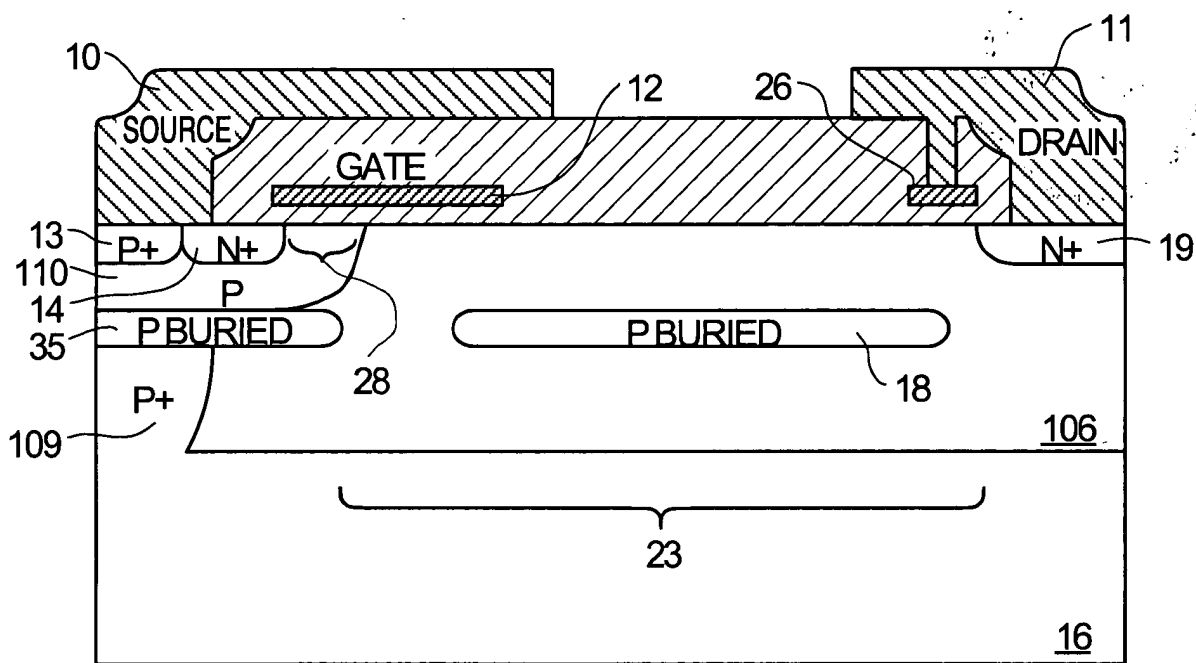


FIG. 5



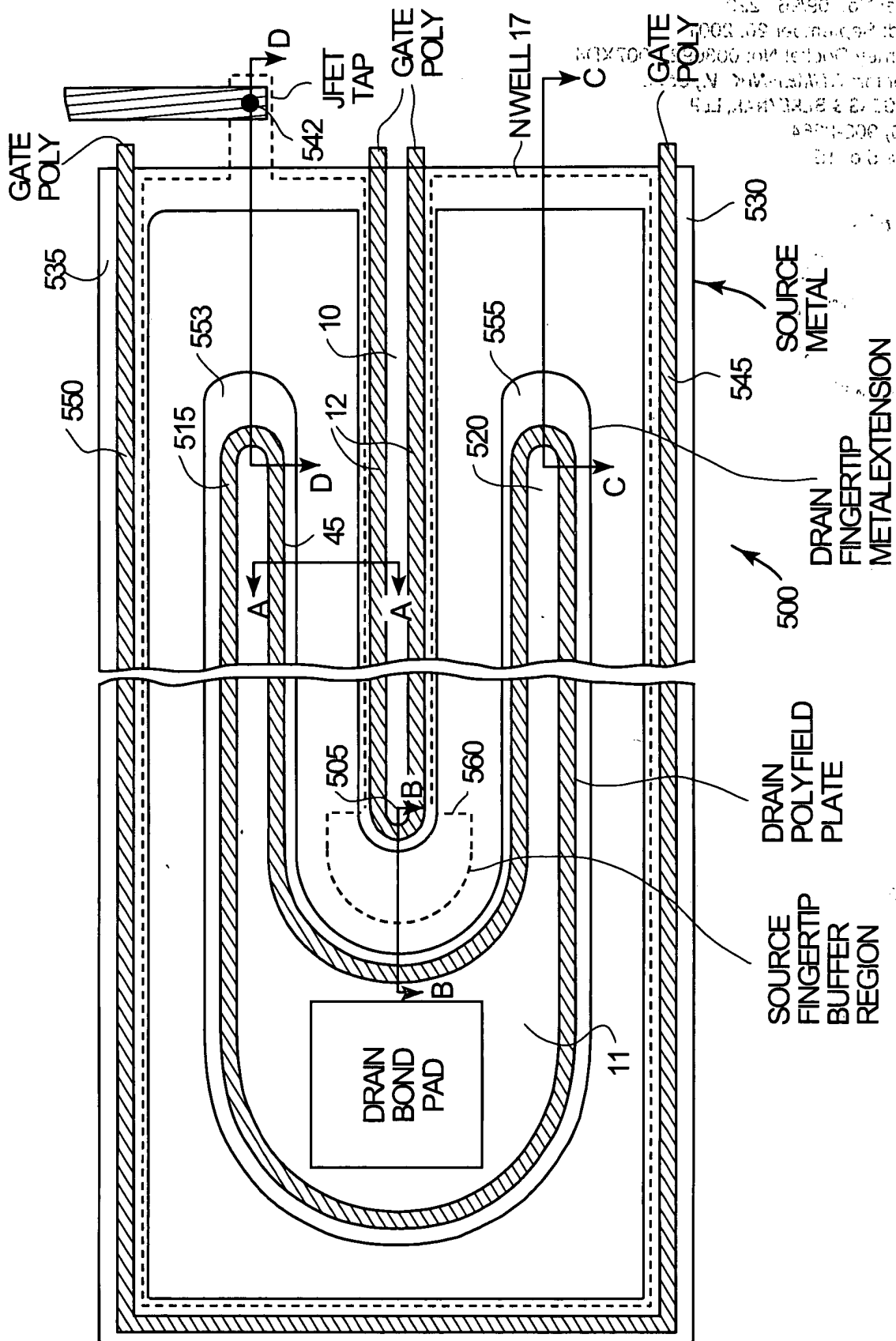


FIG. 7

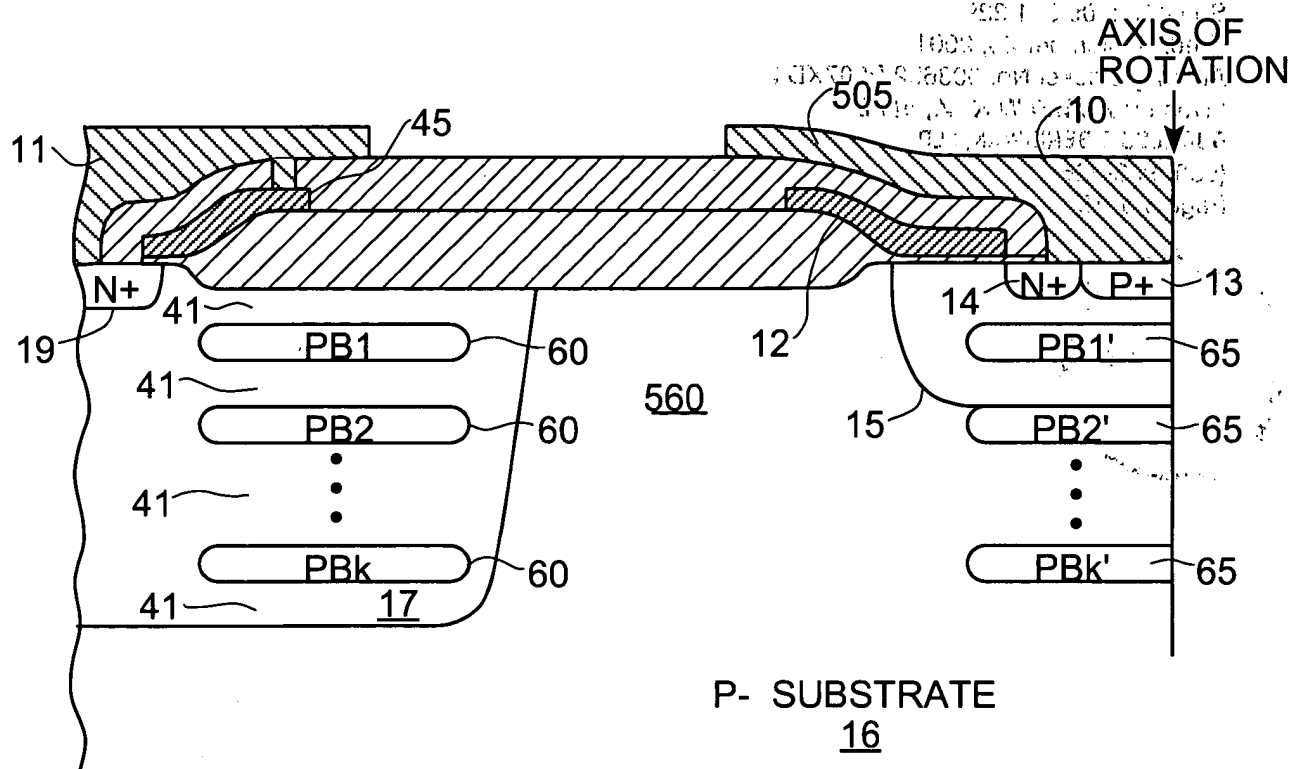


FIG. 8

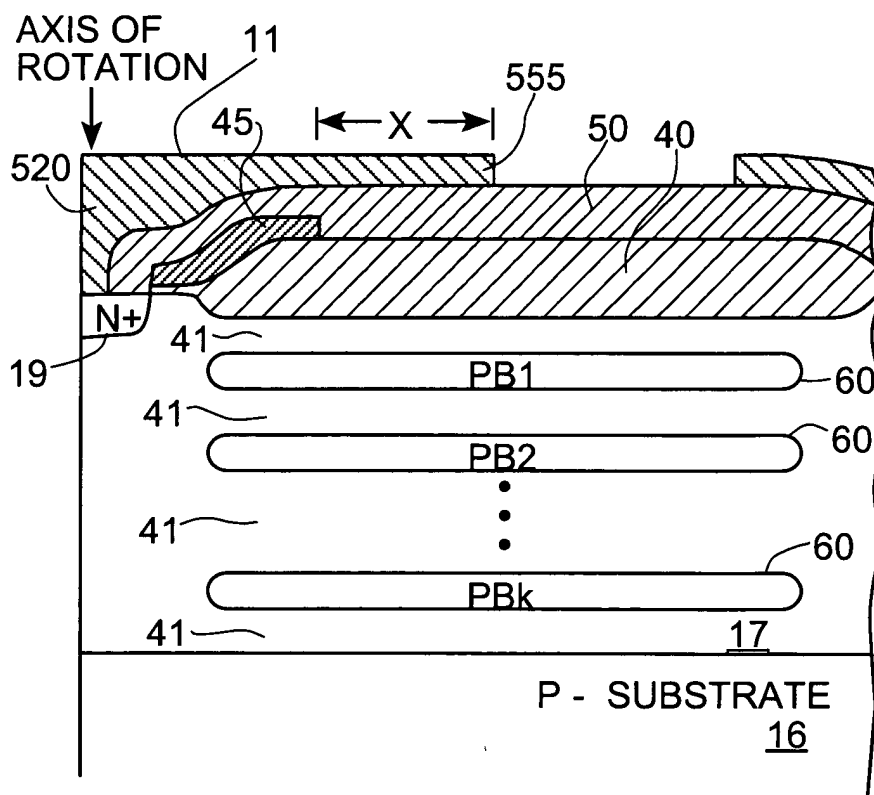


FIG. 9



515

19

N+

41

PB1

60

41

PB2

60

⋮

41

PBn

60

41

17

16

50

TAP METAL

542

700

FIG. 10

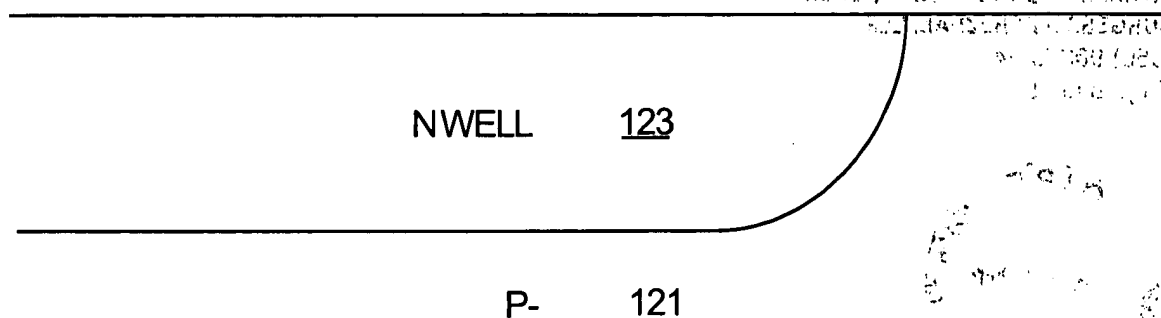


FIG. 11a

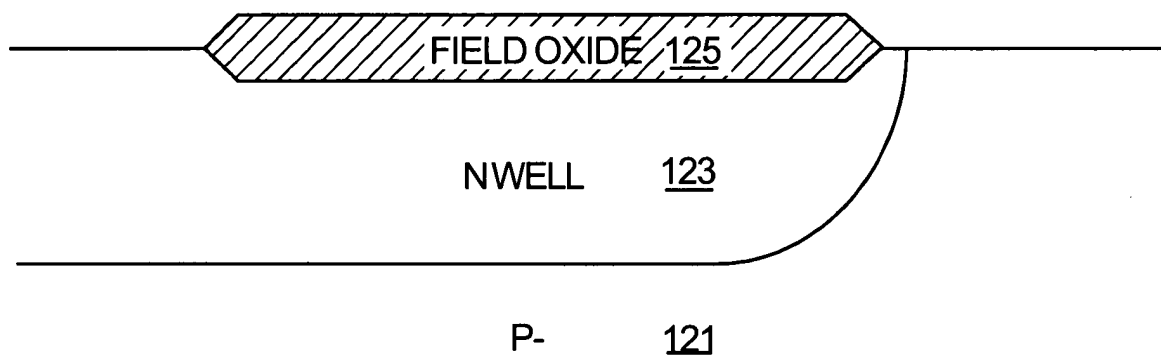


FIG. 11b

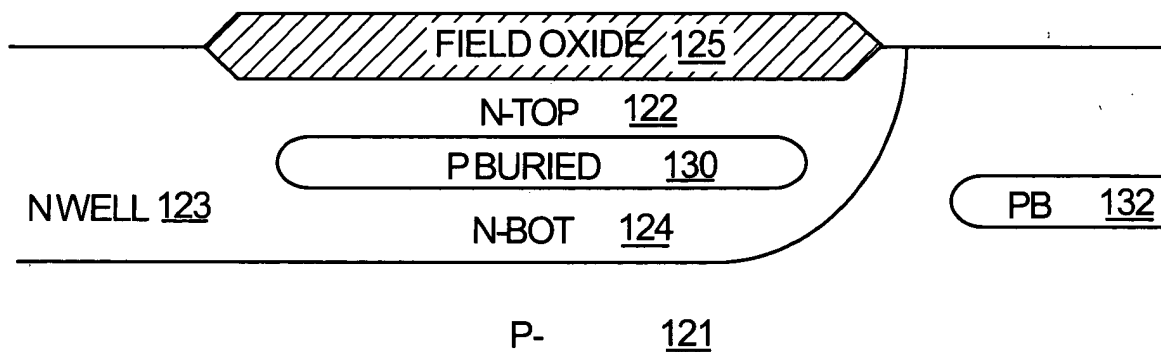


FIG. 11c

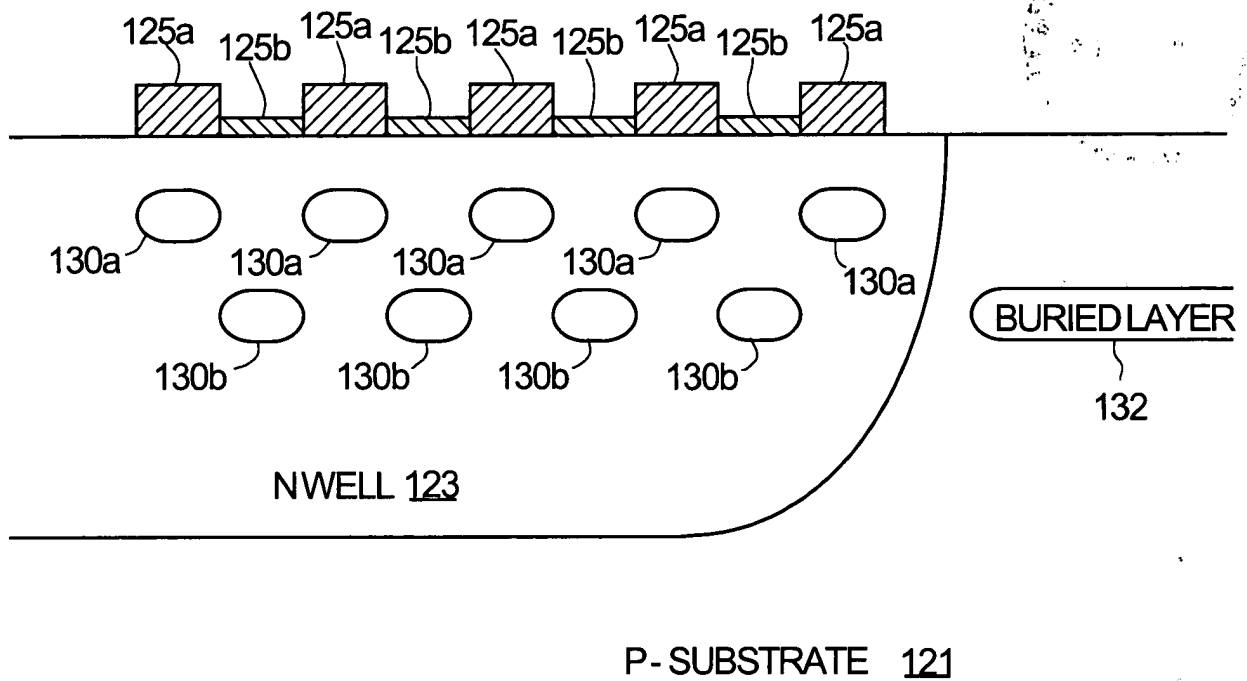


FIG. 11d

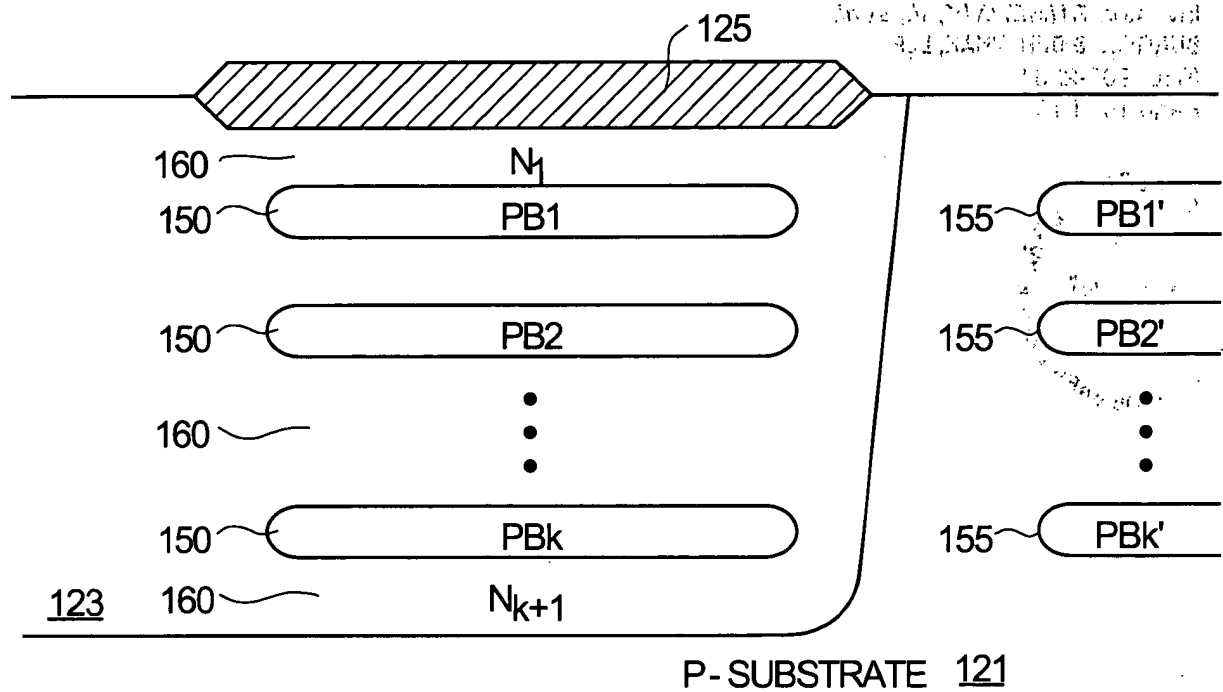


FIG. 11e

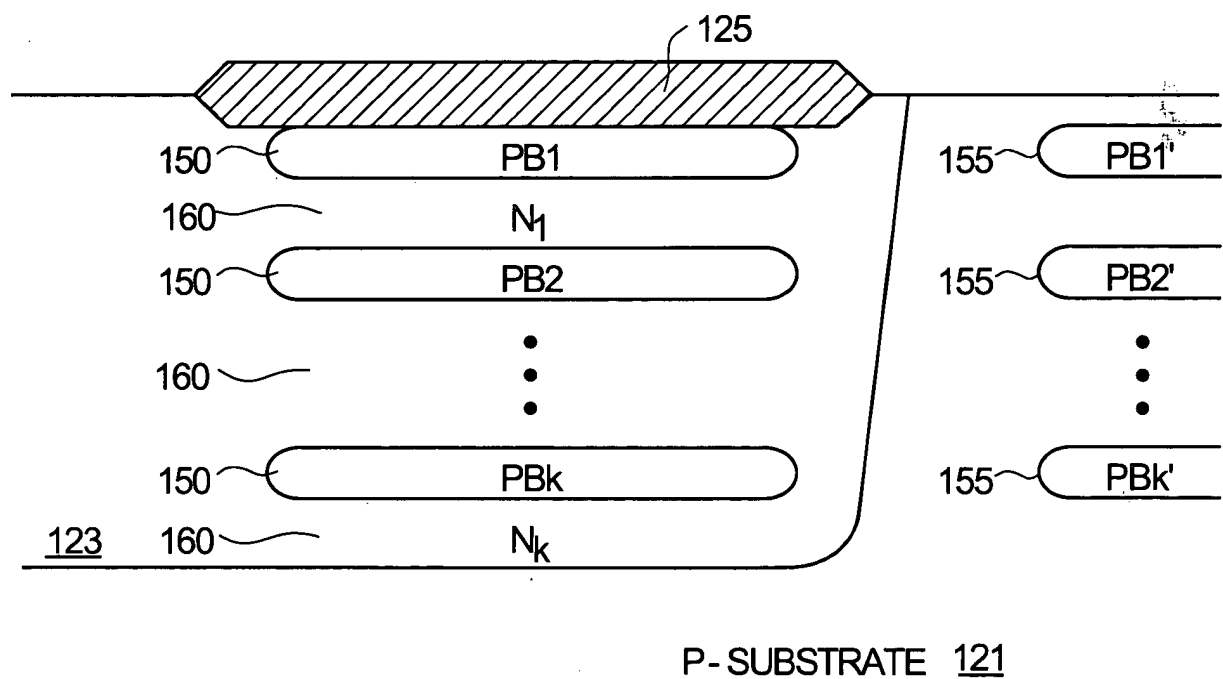


FIG. 11f

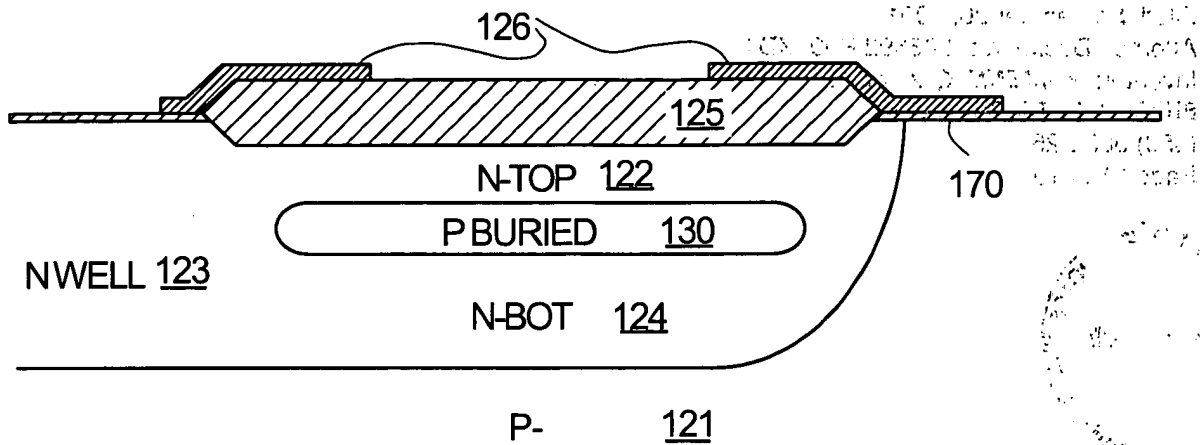


FIG. 11g

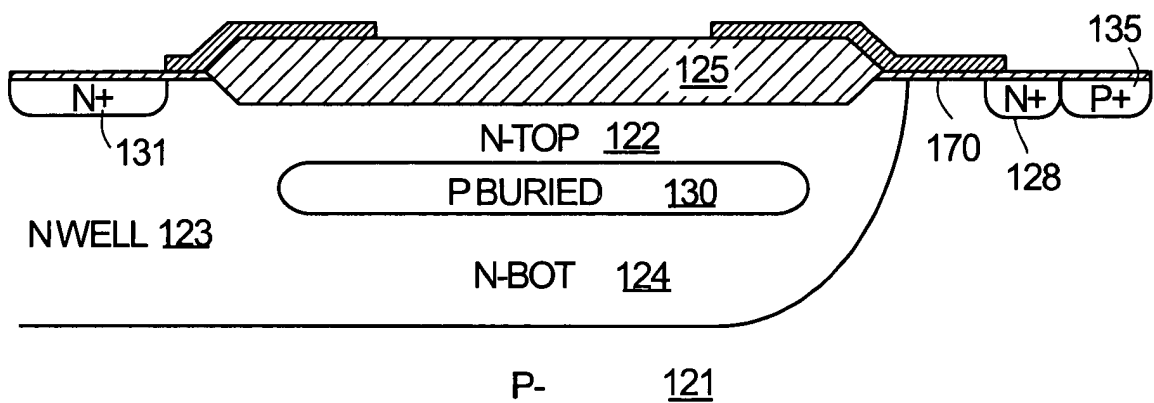


FIG. 11h

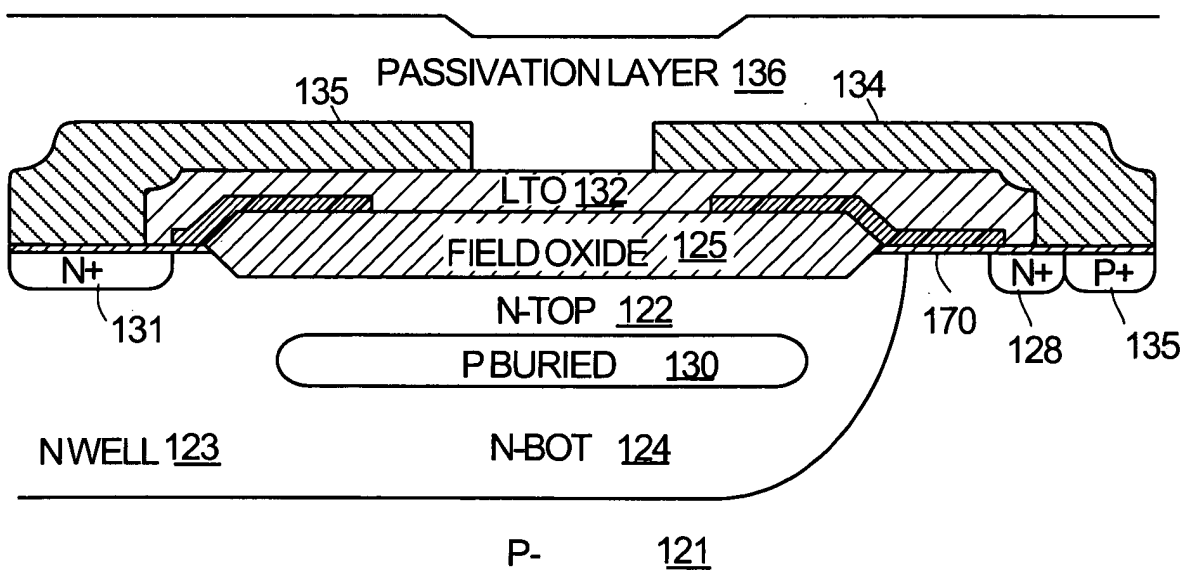


FIG. 11i

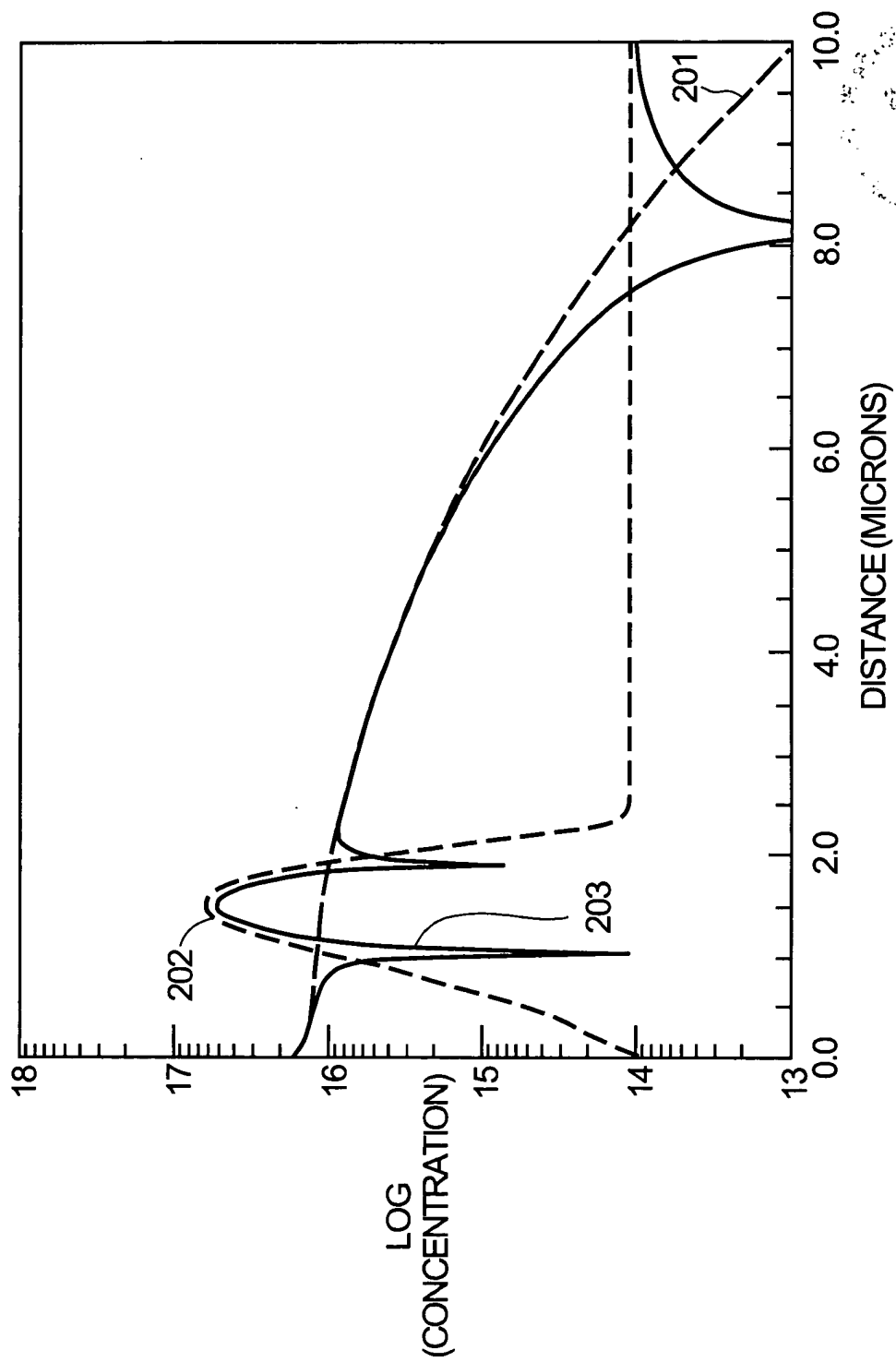


FIG. 12

LOG  
(CONCENTRATION)

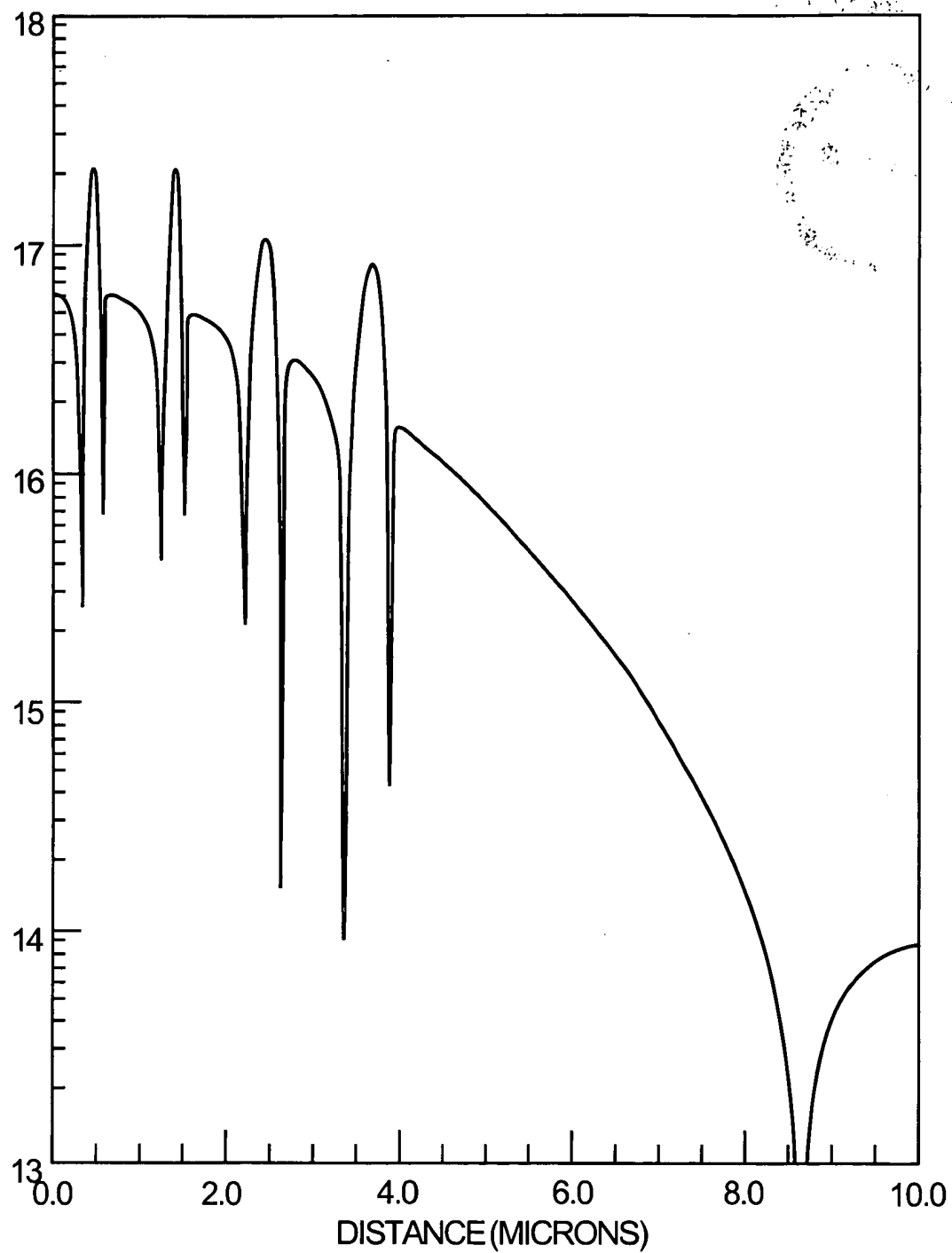


FIG. 13



FIG. 14